CLAIMS

What is claimed is:

1. A device comprising:

a substrate having a plurality of trenches formed therein;

an isolation oxide disposed within each of the plurality of trenches and comprising cavities formed therein along the junction between the substrate and the isolation oxide;

a conductive material disposed in each of the cavities; and

a plurality of doped regions in the substrate arranged directly adjacent to the polysilicon material.

2. The device, as set forth in claim 1, wherein each of the plurality of cavities comprises a depth in the range of approximately 300 angstroms to 1500 angstroms.

3. The device, as set forth in claim 1, wherein each of the plurality of cavities comprises an aspect ratio of less than or equal to approximately 0.5 to 10.

4. The device, as set forth in claim 1, wherein each of the plurality of cavities comprises an aspect ratio of less than or equal to approximately 1 to 3.

5. The device, as set forth in claim 1, comprising a wordline stack disposed directly

over the plurality of doped regions in the substrate.

6. The device, as set forth in claim 5, wherein the wordline stack comprises a polysilicon layer disposed over a field oxide layer.

7. The device, as set forth in claim 5, wherein the conductive material is disposed such that a portion of the conductive material is directly adjacent to a portion of the wordline stack.

8. The device, as set forth in claim 1, wherein the conductive material comprises polysilicon.

9. The device, as set forth in claim 1, wherein the conductive material comprises a metal.

10. The device, as set forth in claim 1, wherein the conductive material comprises a first layer comprising polysilicon and a second layer comprising metal.

11. The device, as set forth in claim 1, wherein the isolation oxide comprises:

a first cavity having a first type of conductive material disposed therein; and

a second cavity having a second type of conductive material disposed therein, wherein the second type is different than the first type.

12. A transistor comprising:

a drain terminal comprising a doped polysilicon material disposed within a first shallow cavity formed in an isolation oxide region;

a source terminal comprising a polysilicon material disposed within a second shallow cavity formed in the isolation oxide region;

a channel formed in a silicon material and arranged between each of the first shallow cavity and the second shallow cavity, wherein the channel comprises a respective doped region coupled to each of the drain terminal and the source terminal; and

a gate disposed over the channel and comprising one or more conductive layers disposed over a gate oxide layer.

13. The transistor, as set forth in claim 12, wherein each of the plurality of cavities comprises a depth in the range of approximately 300 angstroms to 1500 angstroms.

14. The transistor, as set forth in claim 12, wherein each of the plurality of cavities comprises an aspect ratio of less than or equal to approximately 0.5 to 10.

15. The transistor, as set forth in claim 12, wherein each of the plurality of cavities comprises an aspect ratio of less than or equal to approximately 1 to 3.

16. The transistor, as set forth in claim 12, comprising:

a first conductive post coupled to the drain terminal and extending vertically therefrom; and

a second conductive post coupled to the source terminal and extending vertically therefrom;

wherein each of the first and second conductive posts are coupled to the respective drain and source terminals at a distance from the gate that is greater than 50% of the width of the respective drain and source terminals.

17. A memory device comprising:

a storage device; and

a transistor coupled to the storage device, wherein the transistor comprises:

a drain terminal comprising a doped polysilicon material disposed within a first shallow cavity formed in an isolation oxide region;

a source terminal comprising a polysilicon material disposed within a second shallow cavity formed in the isolation oxide region;

a channel formed in a silicon material and arranged between each of the first shallow cavity and the second shallow cavity, wherein the channel comprises a respective doped region coupled to each of the drain terminal and the source terminal; and

a gate disposed over the channel and comprising one or more conductive layers disposed over a gate oxide layer.

18. The memory device, as set forth in claim 17, wherein the storage device comprises a capacitor.

19. The memory device, as set forth in claim 17, wherein each of the plurality of cavities comprises a depth in the range of approximately 300 angstroms to 1500 angstroms.

20. The memory device, as set forth in claim 17, wherein each of the plurality of cavities comprises an aspect ratio of less than or equal to approximately 0.5 to 10.

21. The memory device, as set forth in claim 17, wherein each of the plurality of cavities comprises an aspect ratio of less than or equal to approximately 1 to 3.

22. A system comprising:

a processor; and

a memory device coupled to the processor and comprising:

a storage device; and

a transistor coupled to the storage device, wherein the transistor comprises:

a drain terminal comprising a doped polysilicon material disposed within a first shallow cavity formed in an isolation oxide region;

a source terminal comprising a polysilicon material disposed within a second shallow cavity formed in the isolation oxide region;

a channel formed in a silicon material and arranged between each of the first shallow cavity and the second shallow cavity, wherein the channel comprises a respective doped region coupled to each of the drain terminal and the source terminal; and

a gate disposed over the channel and comprising one or more conductive layers disposed over a gate oxide layer.

23. The system, as set forth in claim 22, wherein each of the plurality of cavities comprises a depth in the range of approximately 300 angstroms to 1500 angstroms.

24. The system, as set forth in claim 22, wherein each of the plurality of cavities comprises an aspect ratio of less than or equal to approximately 0.5 to 10.

25. The device, as set forth in claim 22, wherein each of the plurality of cavities comprises an aspect ratio of less than or equal to approximately 1 to 3.

26. A method comprising:

forming a trench in a substrate;

disposing an isolation oxide into the trench;

forming a first cavity in the isolation oxide along a first edge of the trench;

forming a second cavity in the isolation oxide along a second edge of the trench;

disposing a heavily doped polysilicon into each of the first cavity and the second cavity; and

thermal cycling the substrate such that ions from the heavily doped polysilicon diffuse into the substrate.

27. The method, as set forth in claim 26, wherein forming the trench comprises etching the trench having an aspect ratio of less than or equal to approximately 0.5 to 10.

28. The method, as set forth in claim 26, wherein forming the trench comprises etching the trench having an aspect ratio of less than or equal to approximately 1 to 3.

29. The method, as set forth in claim 26, wherein forming the first cavity and forming the second cavity occur contemporaneously.

30. The method, as set forth in claim 26, wherein disposing a heavily doped polysilicon comprises:

disposing a p-type polysilicon into the first cavity; and

disposing an n-type polysilicon into the second cavity.

31. The method, as set forth in claim 26, wherein thermal cycling comprises thermal cycling at a temperature in the range of approximately 600°C to 1050°C.

32. The method, as set forth in claim 26, wherein thermal cycling comprises thermal cycling for a length of time in the range of approximately 20 to 600 seconds.